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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,943	12/28/2000	Gavin J. Stark	042390.P9926	7954

7590 10/26/2004

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,943	STARK ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Received

2. Receipt is acknowledged of amendment and request for continued examination papers submitted, where the papers have been placed of record in the file.

Claim Objections

3. Claims 13-14 are objected to because of the following informalities: the claims use the acronym ATM, but it is not defined in the claims and thus it's meaning cannot be adequately ascertained. The examiner is interpreting the term ATM to mean asynchronous transfer mode as indicated in the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 8-12, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Slavenburg et al (US Pat. 5,450,556).

6. In regard to claim 1, Slavenburg discloses a processing machine comprising:

a. a data memory (figure 1, element 10);

b. a control engine, linked in communication with the data memory (figure 1, element 15);

c. an instruction memory in which instructions may be stored (figure 1, elements 21 and 22), having an input for receiving control information from the control engine (from element 15); [Column 4, lines 36-40 shows the instruction register 21 store instructions. Column 6, lines 6-33 show that the instruction pipeline 22 incurs a latency from communications with an instruction memory (which may be internal or external block 22).]

d. and a plurality of coprocessors (figure 1, elements 11-14), each connected in communication with the data memory, the instruction memory, and the control engine, the control engine and the plurality of coprocessors coupled to receive a single instruction from the instruction memory in parallel, each of said control engine and plurality of coprocessors being enabled to perform simultaneous functions in response to the single instruction. [Figure 1 shows that the coprocessors 11-14 and control unit 15 each receive a part of a single Very Long Instruction Word (VLIW) stored in instruction register 21 in parallel and perform functions on them. Figure 2, element 50 and column 7, lines 8-13 further show that in fact a single VLIW instruction is stored in instruction register 21.]

7. In regard to claim 2, Slavenburg discloses the processing machine of claim 1, wherein the control engine comprises a microcontroller. [As shown previously and in figure 1, the branch control unit (control engine) receives a control portion of the VLIW instruction. Since the control engine manipulates only a portion of the instruction less than the whole it receives a microinstruction and can be called a microcontroller.]

8. In regard to claim 3, Slavenburg discloses, the processing machine of claim 1, further comprising a main memory linked in communication with at least one of said plurality of coprocessors. [As shown previously, element 22 either contains or is connected with a main memory and thus the coprocessors of figure 1 are also connected to and in communication with the main memory.]

9. In regard to claim 4, Slavenburg discloses the processing machine of claim 3, wherein said at least one coprocessor comprises a bus interface coprocessor. [Elements 13 and 14 of figure 1 are data memory interface coprocessors, which communicate over a bus with the data memory, and are thus bus interface coprocessors.]

10. In regard to claim 5, Slavenburg discloses the processing machine of claim 1, wherein the processing machine is used to perform a particular task and wherein each coprocessor is designated to perform at least one specific subtask of that particular task. [As shown previously, the processor is used to perform the task of a VLIW instruction and the coprocessors perform subtasks according to a smaller portion of the VLIW instruction.]

11. In regard to claim 6, Slavenburg discloses the processing machine of claim 5, wherein the particular task comprises processing a data manipulation algorithm, and specific subtasks performed by separate coprocessors include a memory bus interface function and a data processing algorithm function. [Since an algorithm is simply a set of rules for completing a task, a data manipulation algorithm is performed by the system of figure 1. Further, a data processing algorithm is performed by each of the arithmetic

coprocessors. Elements 13 and 14 of figure 1 are data memory interface coprocessors, which communicate over a bus with the data memory, and are thus memory bus interface coprocessors that perform a memory bus interface function.]

12. In regard to claim 8, Slavenburg discloses a processing machine comprising:

a. a data memory (figure 1, element 10);

b. a main memory (figure 6, element 87);

c. a microcontroller (figure 1, element 15), linked in communication with the data memory; [In figure 1, the branch control unit (control engine) receives a control portion of the VLIW instruction in instruction register 21. Since the control engine manipulates only a portion of the instruction less than the whole it receives a microinstruction and can be called a microcontroller.]

d. an instruction memory in which instructions may be stored (figure 1, elements 21 and 22), having an input for receiving control information from the microcontroller (from element 15), the microcontroller having an input to receive instructions from the instruction memory (from element 21); [Column 4, lines 36-40 shows the instruction register 21 store instructions. Column 6, lines 6-33 show that the instruction pipeline 22 incurs a latency from communications with an instruction memory (which may be internal or external block 22).]

e. a first coprocessor (figure 1, element 13) providing a bus interface function when operational, linked in communication with each of the main memory (via the register file as shown in figure 6), the data memory, and the microcontroller, and having an input to receive instructions from the instruction memory; [Element

13 of figure 1 is a data memory interface coprocessors, which communicates over a bus with the data memory, and is thus a bus interface coprocessor. This coprocessor has communications with the microcontroller since the branch control unit controls the next instructions and thus what the first coprocessor operates on.]

f. and a second coprocessor (figure 1, element 11), linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory, wherein the microcontroller and the first and second coprocessors are coupled to receive the instructions from the instruction memory in parallel (figure 1).

13. In regard to claim 9, Slavenburg discloses the processing machine of claim 8, further comprising: a third coprocessor (figure 1, element 14), linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory (for the same reasons as above).

14. In regard to claim 10, Slavenburg discloses the processing machine of claim 9, further comprising: a fourth coprocessor, linked in communication with the data memory and the microcontroller and having an input to receive instructions from the instruction memory. [As shown in figure 1, the Data Memory Interface coprocessors are numbered 1 through k ad thus any number of these coprocessors is disclosed. Therefore, the 4th coprocessor is another of these interface coprocessors. Connected as given above to meet the limitations of the claim.]

15. In regard to claim 11, Slavenburg discloses the processing machine of claim 8, wherein each of the first and second coprocessors and the microcontroller perform simultaneous coordinated functions in response to a single instruction issued from the instruction memory. [Figure 1 shows that the coprocessors all receive data from a single VLIW instruction and operate simultaneously.]

16. In regard to claim 12, Slavenburg discloses the processing machine of claim 8, wherein the second coprocessor is enabled to process a data manipulation algorithm. [Since an algorithm is simply a set of rules for completing a task, a data manipulation algorithm is performed by the system of figure 1. Further, a data processing algorithm is performed by each of the arithmetic coprocessors including the second coprocessor, element 11.

17. In regard to claim 15, Slavenburg discloses a method of processing a data manipulation task with a processing machine (figure 1) including a control engine (figure 1, element 15) and a plurality of coprocessors (figure 1, elements 11-14), comprising;

a. dividing the data manipulation task into a plurality of subtasks; [As shown in figures 1 and 2 and in column 7, lines 8-13, a VLIW task is divided into a plurality of subtasks.]

b. issuing a sequence of instructions having a plurality of portions to the control engine and each of said plurality of coprocessors; [As shown in figure 1, each VLIW instruction has a plurality of portions that are issued to the control engine and coprocessors.]

c. simultaneously receiving corresponding portions of the instructions in parallel at the control engine and each of said plurality of coprocessors (figure 1);

d. performing separate subtasks with the control engine and each of said plurality of coprocessors by executing the corresponding portions of the instructions received by the control engine and each of said plurality of coprocessors (figure 1);

e. and coordinating the execution of each portion of instructions received by the control engine and each of said plurality of coprocessors such that the subtasks performed by these components are performed substantially in parallel (figure 1).

18. In regard to claim 16, Slavenburg discloses the method of claim 15, wherein the coordination of the execution of the portions of instructions is performed by the control engine via execution control signals sent to each of said plurality of coprocessors. [The branch control unit of figure 1 controls what instructions are executed as shown in the section beginning in column 8, line 60. Each instruction executed at this branch target has a plurality of fields, portions, subtasks, microinstructions, or control signals sent to each coprocessor as shown in figure 1.]

19. In regard to claim 17, Slavenburg discloses the method of claim 16, wherein the processing machine comprises a programmed state machine and wherein each of the control engine and said plurality of coprocessors is caused to cycle through a respective set of machine states in response to instruction portions received by that component. [The summary of the invention shows that the processor (a machine) operates based on

states that are a result of programming. The coprocessors operate according to the programming instructions as shown above and cause them to go through a set (one or more) of states in order to operate on data.]

20. In regard to claim 18, Slavenburg discloses the method of claim 15, wherein one of the subtasks comprises a bus interface function. [The data memory interface coprocessors of figure 1 interface over a bus to the memory and thus perform a subtask specified in the VLIW instruction for this function.]

21. In regard to claim 19, Slavenburg discloses the method of claim 15, wherein the control engine comprises a microcontroller. [As shown previously and in figure 1, the branch control unit (control engine) receives a control portion of the VLIW instruction. Since the control engine manipulates only a portion of the instruction less than the whole it receives a microinstruction and can be called a microcontroller.]

22. In regard to claim 20, Slavenburg discloses the method of claim 15, wherein each instruction is issued from an instruction memory in response to an address sent to the instruction memory from the control engine (column 6, lines 6-32).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Slavenburg.

25. In regard to claim 7,

a. Slavenburg discloses the processing machine of claim 6.

b. Slavenburg does not explicitly disclose wherein the data processing algorithm comprises an encryption algorithm.

c. The Examiner is taking Official Notice that performing an encryption algorithm task on a computer, including a VLIW computer, is conventional and well known in the art.

d. It would have been obvious to one of ordinary skill in the art at the time of invention to perform an encryption algorithm task on the VLIW computer of Slavenburg since the Examiner takes Official Notice that performing an encryption algorithm task on a computer, including a VLIW computer, is conventional and well known in the art and in order to have secure data transfer.

26. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slavenberg in view of Hao (6,028,844).

27. In regard to claim 13,

a. Slavenburg discloses the processing machine of claim 9.

b. While Slavenburg does not explicitly disclose wherein the third coprocessor is enabled to perform an ATM data transfer interface function, Slavenburg does disclose the third coprocessor performing data transfer functions as given above.

c. Hao has disclosed in figure 4 and ATM receiver or coprocessor that performs a data transfer interface function as described in columns 5-7.

d. Hao has disclosed in column 1, lines 26-38 that ATM provides very high-speed transfer rates for an extensive number of services. This high speed and flexibility would have motivated one of ordinary skill in the art to modify the design of Slavenberg to use the ATM data transfer device described in Hao as the third coprocessor (element 13, a data transfer coprocessor) of Slavenburg.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Slavenburg to implement the ATM data transfer device of Hao as the third coprocessor of Slavenberg so that high speed data transfers for a wide range of services are realized.

28. In regard to claim 14,

a. Slavenburg discloses the processing machine of claim 10.

b. Slavenburg does not explicitly disclose wherein the third processor is enabled to perform an ATM data transfer interface function when operational and the fourth processor is enabled to perform an ATM Adaptation Layer (AAL) function when operational. Slavenburg does disclose the third and fourth coprocessors performing data transfer functions as given above.

c. Hao has disclosed in figure 4 and ATM/AAL receiver or coprocessor that performs a data transfer interface function as described in columns 5-7.

d. Hao has disclosed in column 1, lines 26-38 that ATM provides very high-speed transfer rates for an extensive number of services. This high speed and flexibility would have motivated one of ordinary skill in the art to modify the

design of Slavenberg to use the ATM/AAL data transfer device described in Hao as the third and fourth coprocessors (described above) of Slavenburg.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Slavenburg to implement the ATM/AAL data transfer device of Hao as the third and fourth coprocessor of Slavenberg so that high speed data transfers for a wide range of services are realized.

Response to Arguments

29. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents have been cited to further show the art with respect to coprocessors and control engines receiving an instruction in parallel.

US Pat No 6,002,880 teaches a VLIW system where a VLIW instruction is broken into several subtasks and sent to control and coprocessor units simultaneously for processing in addition to the other limitations of the independent claims.

US Pat No 5,974,537 to Mehra discloses a VLIW architecture where a VLIW instruction is divided into several subtasks and sent to control and coprocessor units simultaneously for processing in addition to the other limitations of the independent claims.

Us Pat No 6,044,450 to Tsushima shows a VLIW architecture where a VLIW instruction is divided into several subtasks and sent to control and coprocessor units simultaneously for processing in addition to the other limitations of the independent claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl

Examiner
Art Unit 2183

SFG
October 25, 2004

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